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3	BRS	L4	0	(Micropax and cable) and FPGA	USPAT	2004/07/13 12:21
4	BRS	L2	25	Micropax and cable	USPAT	2004/07/13 12:22
5	BRS	L5	0	Micropax and cable and asynchronous	USPAT	2004/07/13 12:22
6	BRS	L6	0	Micropax near cable	USPAT	2004/07/13 12:23
7	BRS	L7	0	Micropax adj able	USPAT	2004/07/13 12:23
8	BRS	L8	0	Micropax adj cable	USPAT	2004/07/13 12:23
9	BRS	L9	28	logic adj emulator	USPAT	2004/07/13 12:24
10	BRS	L10	0	(logic adj emulator) and Micropax	USPAT	2004/07/13 12:24
11	BRS	L11	0	(logic adj emulator) and Micropax	USPAT; IBM_T DB	2004/07/13 12:24
12	BRS	L12	26	(logic adj emulator) and asynchronous	USPAT; IBM_T DB	2004/07/13 12:25
13	BRS	L13	23546	single adj line	USPAT; IBM_T DB	2004/07/13 12:25
14	BRS	L14	0	L13 and (logic adj emulator)	USPAT; IBM_T DB	2004/07/13 12:26
15	BRS	L15	403	L13 and emulation	USPAT; IBM_T DB	2004/07/13 12:26
16	BRS	L16	74	L13 and emulation and (FPGA)	USPAT; IBM_T DB	2004/07/13 12:46
17	BRS	L17	5	(emulation adj processor) near plurality	USPAT; IBM_T DB	2004/07/13 12:51
18	BRS	L18	0	(emulation adj processor) near plurality and asynchronous	USPAT; IBM_T DB	2004/07/13 12:52

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20	BRS	L20	0	(emulation adj processor) and (asynchronous near card)	USPAT; IBM_T DB	2004/07/13 12:53
21	BRS	L21	0	(emulation adj processor) and (asynchronous near module)	USPAT; IBM_T DB	2004/07/13 13:34
22	BRS	L22	29	Cobalt and emulation	USPAT; IBM_T DB	2004/07/13 13:34
23	BRS	L23	10	Cobalt and emulation and logic	USPAT; IBM_T DB	2004/07/13 13:50
24	BRS	L24	4	Cobalt and emulation and logic and wire	USPAT; IBM_T DB	2004/07/13 13:35
25	BRS	L25	7	asychronous adj clock	USPAT; IBM_T DB	2004/07/13 13:51
26	BRS	L27	0	(asychronous adj clock) and (time same multiplex$) and emulation	USPAT; IBM_T DB	2004/07/13 13:52
27	BRS	L28	2	(asychronous adj clock) and (time same multiplex$) and (cycle-based)	USPAT; IBM_T DB	2004/07/13 13:52
28	BRS	L26	3	(asychronous adj clock) and (time same multiplex$)	USPAT; IBM_T DB	2004/07/13 13:53
29	BRS	L29	0	(asychronous adj clock) and (time same multiplex$) and simulator	USPAT; IBM_T DB	2004/07/13 13:53

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Kudlugi, M.; Tessier, R.;
Computer-Aided Design of Integrated Circuits and Systems, IEEE Transaction on , Volume: 21 , Issue: 11 , Nov. 2002
Pages:1253 - 1268

[Abstract]   [PDF Full-Text (735 KB)]   **IEEE JNL**

2 **Synchronous emulation of asynchronous circuits**
O'Leary, J.; Brown, G.;
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3 **Static scheduling of multiple asynchronous domains for functional verification**
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5 **Asynchronous interlocked pipelined CMOS circuits operating at 3.3-GHz**
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Solid-State Circuits Conference, 2000. Digest of Technical Papers. ISSCC. 20(
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